

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L10	491	((gate or electrode) with stack) and patterning and (ARC or antireflective)	US-PGPUB; USPAT	OR	ON	2005/06/18 16:04
L11	333	10 and removing	US-PGPUB; USPAT	OR	ON	2005/06/18 15:39
L12	318	11 and @ad<"20040318"	US-PGPUB; USPAT	OR	ON	2005/06/18 16:05
L13	14	((gate or electrode) with stack) and patterning and (ARC or antireflective)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/18 15:59
L14	162	((gate or electrode) with stack) and (second adj (area or region or portion)) and (ARC or antireflective)	US-PGPUB; USPAT	OR	ON	2005/06/18 16:04
L15	152	14 and @ad<"20040318"	US-PGPUB; USPAT	OR	ON	2005/06/18 16:05
L16	115	15 not 12	US-PGPUB; USPAT	OR	ON	2005/06/18 16:05
L17	106	16 and only	US-PGPUB; USPAT	OR	ON	2005/06/18 16:05
L18	7	(kuilong adj wang) or (tsengyou adj syau) or (jeong adj choi)	US-PGPUB; USPAT	OR	ON	2005/06/18 16:22
L19	0	(kuilong adj wang) or (tsengyou adj syau) or (jeong adj choi)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/18 16:22

US-PAT-NO: 6894353

DOCUMENT-IDENTIFIER: US 6894353 B2

TITLE: Capped dual metal gate transistors for CMOS process and method for making the same

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Brief Summary Text - BSTX (6):

One problem with the use of metal gates is that most metals are etched when exposed to conventional "pirhana" cleans and SC-1 (Standard Clean-1) cleans. A pirhana clean consists of sulfuric acid, hydrogen peroxide, and water. An SC-1 clean consists of ammonium hydroxide, hydrogen peroxide, and water. These cleans are used throughout the industry to remove photoresist masks used to mask the substrates during various etch, implant and other fabrication steps. More specifically, the problem lies in removing photoresist masks following extension and halo implants for devices having metal gates. These implants are typically performed just after the gates are patterned and etched. In removing the photoresist implant masks, the piranha or SC-1 solutions attack the metal gates as well.

Drawing Description Text - DRTX (5):

FIG. 3 is a partial cross sectional view subsequent to FIG. 2 in which a second gate metal, a polysilicon capping layer, and an ARC are deposited over the first gate metal;

Detailed Description Text - DETX (4):

The polysilicon capping layer was also found to be beneficial in protecting the sides of the gate structure. A problem discovered by Applicants in using zero layer spacers alone, or zero layer spacers in conjunction with an overlying ARC (anti-reflective coating) on the gates, is that topographical variations across the wafer surface made it very difficult to control the zero layer spacer etch. The zero layer spacer etch is more or less a timed etch because the etch is not sufficiently selective to the underlying gate dielectric material. With topographical variations across the wafer (e.g. active regions versus isolation regions), a great deal of variation in the spacer protection of the gate structures was observed. For example, while the spacers sufficiently protected sidewalls of the gates in the active region, where these gate metals crossed over isolation regions the metal sidewalls may

be exposed and attacked during removal of photoresist masks. By employing a polysilicon cap on top of the gate structure there is much greater tolerance (process margin) for the variability of zero layer spacers.

Detailed Description Text - DETX (5):

Further benefits of using the polysilicon capping layer include the ability to contact the gate electrode without a separate etch step previously needed to open or etch the ARC formed on the gate. With the present invention, the ARC layer can be removed immediately after patterning the gates because it is not needed as a protecting layer during etches (the polysilicon cap serves this function). Furthermore, the polysilicon cap readily enables silicidation of the gates with the source/drain regions of the device in a self-aligned manner.

Detailed Description Text - DETX (14):

Preferably second metal 114 is deposited to approximately the same thickness as first metal 110, with each metal layer being in the range of 50-1000 angstroms (5-100 nanometers) thick. Silicon containing layer 116 is preferably deposited to a thickness in the range of 100-1500 angstroms (10-150 nanometers). The silicon containing layer thickness is not critical, but the thicker it is the more margin there will be in a subsequent spacer formation process, as described below. The thickness of the silicon containing layer can be the variable thickness layer of the gate stack. In other words, if a particular gate structure should be limited or targeted to a particular total thickness, the silicon containing layer can be the layer whose thickness is varied to achieve that thickness.

Detailed Description Text - DETX (15):

Keeping with FIG. 3, an anti-reflective coating (ARC) 118 is deposited over silicon containing layer 116. ARC 118 is preferably a silicon-rich silicon nitride layer, although any ARC material which serves an ARC function for the particular lithography process used is suitable. In a preferred embodiment, the ARC is deposited by conventional techniques to about 200 angstroms (20 nanometers) thick.

Detailed Description Text - DETX (16):

Turning now to FIG. 4, semiconductor device 100 is depicted after a gate mask and etch process have been performed to pattern first metal layer 110, second metal layer 114, and silicon containing layer 116, resulting in the formation of a first gate 120 over first well 104 and a second gate 122 over second well 106. First gate 120 includes a first metal 110 on gate dielectric 108 and a second metal 114 formed on first metal 110. In contrast, second gate 122 includes second metal 114 in contact with gate dielectric 108. Both the

first gate 120 and second gate 122 have an overlying cap formed of silicon containing layer 116. ARC layer 118 is initially also patterned during the gate stack etch but it can be fully removed after the gate etch, and thus is not shown in FIG. 4. Because silicon containing layer 116 serves to protect the metal gates during subsequent etches and cleans, there is no need to keep an ARC layer on top of the gates. This is advantageous in that the ARC need not later be separately etched during a contact etch process to form a contact to the gate, and instead can be wet etched. Furthermore, complete removal of the ARC enables a more robust silicidation process on top of the gate.

Detailed Description Text - DETX (17):

In accordance with one embodiment of the invention wherein first metal 110 is TiN and the second metal 114 is TaSiN, the following etch was found suitable to form the gate stack without deleterious affects on the silicon containing layer 116 and gate dielectric 108. A silicon-rich silicon nitride as ARC 118 is first patterned using a plasma etch with a CF.sub.4 /Ar chemistry. A polysilicon layer for silicon containing layer 116 is then patterned using a plasma etch of a Cl.sub.2 /HBr chemistry. Thereafter, the TaSiN is patterned using a plasma etch with a CF.sub.4 /Ar chemistry similar to that used to etch through the ARC. This etch passivates the patterned polysilicon by formation of a polymer sidewall on exposed portions of the polysilicon. Because the gate dielectric 108 over second well 106 may not serve as a full etch stop, and to minimize the damage to gate dielectric 108 in this region, the bias power (i.e. the bias on the wafer) is preferably reduced near the end of the etch of the TaSiN layer. When to reduce the power can be readily determined experimentally. After clearing the TaSiN, the TiN is patterned using a plasma etch chemistry using Cl.sub.2 and He. An important aspect of etching metal 110 is to minimize exposure of gate dielectric 108 to the etch chemistry in the region of second gate 122 and second well 106 so that the gate dielectric is not removed in this area. Removal of the gate dielectric may result in etching or trenching of the underlying silicon in second well 106. To avoid damage to the gate dielectric, the ratio of the source bias to the substrate bias used during the etch of TiN can be significantly increased relative to conventional TiN etching, together with a reduced chamber pressure. As such, the TiN is etched very fast and therefore exposure of the gate dielectric in the other portion of the device to the etch is minimized. As an example, a suitable ratio of source bias to substrate bias may be about 33:1, as compared to 2:1 which is more typically used in conventional TiN etching. The chamber pressure, for example, could be reduced from 40 millitorr (mT), which is conventionally used, to 10 mT.

Detailed Description Text - DETX (18):

Continuing with FIG. 4 after patterning first gate 120 and second gate 122, first spacers 124 are formed along sides of both gates. In a preferred embodiment, first spacers 124 are formed by depositing a thin layer of silicon nitride (100-300 angstroms or 10-30 nanometers) and then anisotropically etching the wafer so that the silicon nitride is left only along the sidewalls of the gates. As a result of the etch, the resulting spacers will have tapered shaped, as shown in FIG. 4, having a maximum thickness or width near the bottom each gate of about 50-200 angstroms (5-20 nanometers). First spacers 124 serve to protect the metal gates from being etched during subsequent removal of an implant mask. As mentioned previously, conventional piranha and SC-1 cleans used to strip photoresist masks also attack many metals being proposed for metal gates.

Detailed Description Text - DETX (19):

As illustrated in FIG. 4, the height of first spacers 124 relative to the total height or thickness of the gates may vary. For example, first spacers 124 rise higher along the sidewall of second gate 122 as compared to first gate 120. This is not a problem because the presence of silicon containing layer 116 provides sufficient protection for the metal, gates during subsequent etches because silicon containing layer 116 is resistant to attack from these etches. Thus, the process has a large process margin for variations in topography and gate stack heights due the presence of silicon containing layer 116. As long as the spacers cover all of the sidewalls of the underlying metals beneath silicon containing layer 116, the gate stack will be adequately protected.

Detailed Description Text - DETX (24):

As illustrated in FIG. 6, layer 136 is anisotropically etched to form second spacers 138 without completely removing oxide liner 134. This can be accomplished with a combination of silicon dioxide and silicon nitride and using a conventional dry etch chemistry of CF₄, HBr and Ar. The oxide liner 134 may be thinned during formation of spacers 138, but this is not detrimental as long as the underlying substrate material (e.g. silicon) is not exposed at this point in the process.

Detailed Description Text - DETX (26):

Now in reference to FIG. 7, an anneal is next performed to diffuse the extension and source/drain regions to the desired profile and to activate the dopants. Again, this is done using conventional practices. Thereafter, remaining portions of the oxide liner 134 are removed from unprotected regions of the device (e.g. from above the source/drain regions, the gates, and the isolation regions) using a conventional wet etch. The exposed source/drain

regions and gates are then silicided using a self-aligned process by, for example, depositing a blanket layer of titanium, cobalt or nickel and thermally reacting this metal with the adjacent silicon regions to form silicide regions 144 as shown in FIG. 7. Thus, there is little deleterious affect in using a silicon containing cap over first gate 120 and second gate 122 from a resistance perspective because the silicidation process used to silicide the source/drain regions can be used to silicide the gate at the same time for satisfactory resistance levels. Resistance can be further reduced by completely siliciding the silicon containing layer 116 in the gate stack provided the silicided regions above the source/drain regions and the source/drain regions themselves are adjusted as may be needed.

Detailed Description Text - DETX (28):

By now it should be apparent that there has been providing a capped dual metal gate structure for use in a CMOS process which overcomes the problems previously described. More specifically, the present invention provides a reliable method for forming a dual gate metal structure using a silicon containing cap layer and zero spacers (first spacers 124) which renders the gate stack resistant to conventional piranha and SC-1 cleans used to remove photoresist masks following halo and extension implants. The cap and spacers expand the process window so that the process is reliable even with topographical variations across the wafer surface. The silicon containing cap also eliminates the need to keep an ARC layer on the gate through contact etch, and therefore eliminates the need to separately etch the ARC during the contact etch process. The silicon containing cap thickness is also scalable, allowing it to be varied to match the particular targeted gate stack height. A further advantage of the invention is that it can be implemented independent of the choice of metals and gate dielectrics used to form the gate stacks. Moreover, use of the silicon containing cap allows the use of more conventional self-aligned silicide processes, wherein the gate and the source/drain regions are silicided at the same time.

Detailed Description Text - DETX (29):

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, although the invention has been described with respect to specific conductivity types or polarity of potentials, skilled artisans appreciated that conductivity types and polarities of potentials may be reversed. Additionally, the invention can be extended to form three or more gate stacks with different metal gate materials. For example, in addition to

having a gate stack which includes one metal capped with a silicon containing layer and a gate stack which includes two metals capped with a silicon containing layer, there could be a third gate stack which includes three metals capped with a silicon containing layer. The third gate stack may be advantageous for forming the input/output transistors of a device that typically have higher threshold voltage requirements than logic transistors. A third gate stack could be achieved by depositing and patterning the first metal layer, as shown in FIG. 2, then depositing a second metal and patterning it similarly over the area for the second gate stack. Then depositing the third metal layer and the silicon containing capping layer as shown in FIG. 3. This can further be extended similarly to form a fourth gate stack, a fifth gate stack, etc. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

US-PAT-NO: 6835662

DOCUMENT-IDENTIFIER: US 6835662 B1

TITLE: Partially de-coupled core and periphery gate module
process

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Abstract Text - ABTX (1):

The invention is an apparatus and a method of manufacturing a structure. The method includes the step of patterning a layer to include a line and space pattern. A space of the line and space pattern in a first region includes a first critical dimension less than achievable at a resolution limit of lithography. A line of the line and space pattern in a second region includes a second critical dimension achievable at a resolution limit of lithography. A sidewall spacer is formed on a line from a masking layer used in the formation of the structure. The method uses one critical masking step and two non-critical masking steps.

Brief Summary Text - BSTX (8):

According to one aspect of the invention, the invention is a method of forming a layer comprising a line and space pattern over a substrate including a first region and a second region, the method comprising the steps of: depositing and patterning a first hard mask layer over the layer to form a master line and space pattern therein, wherein a first master line and space pattern in the hard mask layer includes at least one line and at least one space of a minimum dimension dictated by a resolution limit of lithography; etching the layer to form the line and space pattern in the second region corresponding to the first master line and space pattern in the hard mask layer in the second region, wherein a line in the second region includes a first critical dimension (B) achievable at the resolution limit of lithography; depositing a second hard mask layer over the patterned first hard mask layer, etching the second hard mask layer to form sidewall spacers on sidewalls of at the least one line in the hard mask layer in the first region, wherein the minimum dimension of the at least one space in the first hard mask layer in the first region is reduced to a second critical dimension (A) less than achievable at the resolution limit of lithography; to form sidewall spacers on sidewalls of the at least one line in the second region; and etching the layer to form the line and space pattern in the first region corresponding to the first

master line and space pattern in the hard mask layer in the first region, wherein a space in the first region includes the second critical dimension (A) less than achievable by the resolution limit of lithography.

Brief Summary Text - BSTX (9):

According to another aspect of the invention, the invention is a method of **patterning** a layer on a substrate including a first region and a second region, the method comprising the steps of: providing a substrate including the layer to be patterned interposed between the substrate and a first hard mask layer to be patterned; coating the first hard mask layer to be patterned with a first photosensitive layer; **patterning** and etching the first photosensitive layer to form a first patterned image including lines and at least one space, the lines in the first photosensitive layer and the at least one space include substantially vertical walls and include a minimum dimension (B) achievable at a resolution limit of lithography; transferring to the first hard mask layer the first patterned image by anisotropically etching the first hard mask layer to form lines and at least one space, the lines and the at least one space in the first hard mask layer include substantially vertical walls and the minimum dimension (B) achievable at the resolution limit of lithography; coating the first hard mask layer with a second photosensitive layer; **patterning** and etching the second photosensitive layer to form a second patterned image including a mask over the first region and exposing the second region; etching the layer in the second region to form a line and space pattern therein including at least one line in the second region including the critical dimension (B) achievable at the resolution limit of lithography; depositing a conformal hard mask layer over the hard mask layer, exposed surfaces of the layer and exposed surfaces of the substrate; forming sidewall spacers on the vertical walls of the lines of the first hard mask in the first region whereby the minimum dimension (B) of the at least one space in the first region is reduced; forming sidewall spacers on the vertical walls of the at least one line in the second region; coating the substrate with a third photosensitive layer; **patterning** and etching the third photosensitive layer to form a third patterned image, wherein the first region is exposed and a remaining portion of the third photosensitive layer acts as a mask in the second region; etching the layer in the first region to form a line and space pattern, wherein the at least one space in the layer in the first region includes a second critical dimension (A) less than achievable by the resolution limit of lithography.

Detailed Description Text - DETX (5):

Additionally, a sidewall spacer (e.g., a transistor spacer) may be formed on the sidewalls of a line in the second region. The sidewall spacer is formed from a second mask layer used in forming the hard mask for **patterning** the layer

in the core region. The line in the second region may be a gate electrode of a gate, for example.

Detailed Description Text - DETX (7):

The present invention includes a method of patterning a layer comprising varying pitch and at least two critical dimensions that also results in the formation of a transistor spacer from a second mask layer used in forming a master hard mask for patterning of the layer. The method uses one critical masking step and two non-critical masking steps to pattern the layer. The method includes a step of forming the layer on or over a substrate or wafer including at least two regions, e.g., a first region and a second region.

Detailed Description Text - DETX (12):

Thus, the space between the core gates includes a lateral dimension less than achievable at a resolution limit of lithography. Further, the periphery gates include a lateral dimension achievable at a resolution limit of lithography. Further still, the periphery gates include sidewall spacers formed from the second mask layer used in forming the master hard mask used in patterning the conductive layer in the core region. The semiconductor device resulting from the method includes significantly increased performance while being produced at significantly reduced manufacturing costs.

Detailed Description Text - DETX (13):

Starting with a substrate (e.g., semiconductor, insulator or metal) including a first region and a second region, a layer to be patterned is formed over the substrate. Next, a first mask layer of, for example, an insulator material, such as silicon oxide (Si.sub.x O.sub.y), is formed on the layer to be patterned. In one embodiment, the first mask layer includes a high temperature oxide (HTO). In one embodiment, an anti-reflective coating (ARC) of silicon rich nitride (SiRN), for example, is deposited on the first mask layer. Then, a first layer of photosensitive material is applied. The first layer of photosensitive material is patterned by lithographic means to form a first lithographic image. The first lithographic image includes lines and spaces in the first layer of photosensitive material in the first region and the second region. The lines and spaces include a minimum dimension achievable at a resolution limit of lithography.

Detailed Description Text - DETX (18):

Another etch process, for example, another RIE using a different etchant species, is used to remove portions of the second mask layer from the horizontal surfaces of the first hard mask (and/or ARC, if used) and portions of the horizontal surfaces of the layer exposed by the spaces. The RIE leaves

portions of the second mask layer on the non-horizontal surfaces corresponding to the sidewalls of the lines in the first hard mask in the first region, also referred to herein as hard mask spacers. Thus, the master hard mask is formed. The master hard mask includes the first master line and space sub-pattern formed over the first region. Additionally, sidewall spacers are formed on the sidewalls of the lines in the second region, also referred to herein as transistor spacers of hard mask material.

Detailed Description Text - DETX (19):

The ARC exposed by the etch process in the first and second regions may be removed by another etch process selective to the ARC. Alternatively, an ARC strip may be performed to remove the remaining ARC material. It should be understood by those having ordinary skill in the art that removal of the ARC at this time is optional. If the ARC is not removed, then the ARC functions as part of the master hard mask.

Detailed Description Text - DETX (24):

Following such use, the new mask may be removed from the horizontal surfaces of the layer by subjecting the new mask to a wet or dry etchant. The sidewall spacer formed on the sidewall of a gate in the second region is reduced in size accordingly. If the structure includes at least one gate stack structure of a typical gate, e.g., metal on semiconductor field effect transistor (MOSFET), floating gate (FG), semiconductor oxide-nitride-oxide semiconductor (SONOS) gate or the like, then conventional processes may be used to complete the semiconductor device(s). Those with ordinary skill in the art will understand additional spacers, wordlines, bitlines, contacts, and source and drain regions, for example, may be formed to complete a working device. For brevity sake and to focus on the inventive aspects of the present invention, the features and the processes associated with the formation of such features will not be further discussed in the present application.

Detailed Description Text - DETX (28):

The semiconductor device 10 may include gates comprising conventional gate stack structures. For example, a SONOS gate structure is illustrated in the first region 14. The SONOS gate structure includes a dielectric layer 22a, e.g., an oxide-nitride-oxide (ONO) layer, interposed between the gate electrodes 18a and 18b and the substrate 12. A MOSFET structure is illustrated in the second region 16. The MOSFET structure includes a dielectric layer 22b interposed between the gate electrodes 18c and 18d and the substrate 12. Alternatively, a floating gate structure, including a dielectric layer, a charge-rapping layer, an ONO layer and a control gate may be formed (not shown).

Detailed Description Text - DETX (38):

Further, the method forms a semiconductor device 10 which saves processing steps by using one critical masking step and two non-critical masking steps in the formation of the line and space pattern 20 in the layer 18. The method also forms a multi-use spacer 28a from a hard mask layer used in the formation of a master hard mask used in the patterning of the layer 18, for example. That is, the simultaneous masking of the core and periphery gates, e.g., polysilicon layer, using the single critical mask eliminates the need to reduce a printed periphery critical dimension in order to account for a hard mask spacer formed on a hard mask in a conventional process. Additionally, the single process for forming the small core space(s) and the periphery spacer saves processing steps. For example, the periphery spacer may be used as an implant spacer. Additionally, very small spaces can be formed in the core region without the use of lithography to print the very small spaces. Also, the method extends the use of current lithography apparatuses. Thus, core and periphery gates with faster operating speeds may be achieved. Further, the cost of manufacturing the semiconductor device can be reduced.

Detailed Description Text - DETX (60):

Next, an anti-reflective coating (ARC) 40 is applied. The ARC 40 is optional. However, the ARC 40 is used when increased resolution of the lithography process is required. The ARC 40 material may also comprise at least one of silicon oxide, Si.sub.x O.sub.y , silicon-dioxide (SiO.sub.2), silicon rich oxide (SiRO), other oxides; silicon nitride (Si.sub.x N.sub.y), SiRN , oxygen rich nitride, other nitrides; silicon carbide (Si.sub.x C.sub.y), other carbides; amorphous carbon, spin on organic ARC material; the aforementioned materials implanted with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in porous, amorphous or nanocrystalline form; and mixtures thereof.

Detailed Description Text - DETX (61):

For illustrative purposes, the ARC 40 comprises silicon rich nitride (SiRN) applied, for example, by CVD. The ARC 40 may have a thickness in the range of about 30 nm to about 50 nm, for example.

Detailed Description Text - DETX (62):

Next in Step 216, a first photosensitive layer 42 of a photosensitive material is applied over the ARC 40, for example, by spin-coating. The first photosensitive layer 42 may have a thickness in the range of about 30 nm to about 50 nm, for example. The first photosensitive layer 42 is a photoresist selective to the first hard mask layer 38 or the ARC 40, if an ARC is used.

That is, the photoresist is compatible with the first hard mask layer 38 and when processed, can be used as an etch mask to etch a lithographic image into the first hard mask layer 38.

Detailed Description Text - DETX (66):

Next, in Step 224, as illustrated in FIG. 4, an anisotropic etch is conducted to transfer the lithographic image of the patterned sub-first photosensitive layers 42a-42d to the first hard mask layer 38. An etchant removes the ARC 40 exposed by the openings 44. Further, the etchant removes the first hard mask layer 38 beneath the exposed ARC 40. The etch step leaves openings 46, including the lateral dimension B, in the patterned first hard mask layer 38. In one embodiment, the line/space ratio may be, for example, from about 0.07 μm /0.09 μm . In another embodiment, the line/space ratio may be, for example, from about 0.10 μm /0.15 μm . In another embodiment, the line/space ratio may be, for example, from about 0.12 μm /0.19 μm . In other words, for a specific pitch, e.g., 160 nm, 250 nm or 310 nm, a line is about 40% of the pitch.

Detailed Description Text - DETX (67):

The resultant structure includes a first vertical stack and a second vertical stack in the first region 14 and a third vertical stack and a fourth vertical stack in the second region 16. The first vertical stack includes a sub-first hard mask layer 38a, a sub-ARC layer 40a and a sub-first photosensitive layer 42a. The second vertical stack includes a sub-first hard mask layer 38b, a sub-ARC layer 40b and a sub-photosensitive layer 42b. The third vertical stack includes a sub-first hard mask layer 38c, a sub-ARC layer 40c and a sub-first photosensitive layer 42c. The fourth vertical stack includes a sub-first hard mask layer 38d, a sub-ARC layer 40d and a sub-first photosensitive layer 42d.

Detailed Description Text - DETX (71):

Referring now to FIG. 5, the second photosensitive layer 50 is patterned by pattern-exposing using a conventional lithographic tool, developed, rinsed and dried as described above. That is, the second photosensitive layer 50 is patterned to form a protective mask over the first region 14, i.e., a sub-second photosensitive layer 50a, and to expose the second region 16 by removing a portion of the second photosensitive layer 50 over the second region 16.

Detailed Description Text - DETX (73):

The resultant structure is shown in FIG. 6. The resultant structure includes a fifth vertical stack and a sixth vertical stack in the second region

16. The fifth vertical stack includes the gate electrode 18c, a sub-first hard mask layer 38c and a sub-ARC layer 40c. The sixth vertical stack includes the gate electrode 18d, a sub-first hard mask layer 38d and a sub-ARC layer 40d. The fifth vertical stack and the sixth vertical stack hereinafter may also be referred to as lines 52.

Detailed Description Text - DETX (75):

Referring now to Step 236, FIG. 7, sidewall spacers are formed on the vertical surfaces 48 of the sub-first hard mask layers 38a and 38b and the sub-ARC layers 40a and 40b in the first region 14 to reduce by a lateral dimension C (FIG. 8) the openings 46 (FIG. 5). Additionally, sidewall spacers are formed on the vertical surfaces of the lines 52 in the second region 16 to produce transistor spacers, implant spacers or the like.

Detailed Description Text - DETX (79):

The lower limit for the thickness of the conformal second hard mask layer 28 is dictated by the requirements of good step coverage associated with the substantially vertical wall profile in the first hard mask layer 38, including the ARC 40, and the viability of the conformal second hard mask layer 28 as a thin layer. The upper limit for the thickness of the conformal second hard mask layer 28 is determined by the desired percentage reduction in the size of the opening 46 in the first hard mask layer 38.

Detailed Description Text - DETX (81):

Next, in Step 240, the conformal second hard mask layer 28 is anisotropically etched to remove it from all the substantially horizontal surfaces of the sub-ARC layers 40a-40d and portions of the layer 18 leaving it only on the substantially vertical surfaces of the sub-first hard mask layers 38a-38d, the sub-ARC layers 40a-40d and the lines 18c and 18d. Next, an optional ARC strip is done to remove the remaining ARC 40 (sub-ARC 40a-40d) in both the first region 14 and the second region 16.

Detailed Description Text - DETX (89):

The resultant structure includes a seventh and an eighth vertical stack in the first region 14. The seventh and eighth vertical stacks include the gate electrode 18a, a sub-first hard mask layer 38a and a sub-ARC layer 40a. The eighth vertical stack includes the gate electrode 18b, a sub-first hard mask layer 38b and a sub-ARC layer 40b. The seventh vertical stack and the eighth vertical stack include a space 24 therebetween.

Claims Text - CLTX (1):

1. A method of forming a layer comprising a line and space pattern over a

substrate including a first region and a second region, the method comprising the steps of: depositing and **patterning** a first hard mask layer over the layer to form a master line and space pattern therein, wherein a first master line and space pattern in the first hard mask layer includes at least one line and at least one space of a minimum dimension dictated by a resolution limit of lithography; etching the layer to form the line and space pattern in the second region corresponding to the first master line and space pattern in the first hard mask layer in the second region, wherein a line in the second region includes a first critical dimension (B) achievable at the resolution limit of lithography; depositing a second hard mask layer over the patterned first hard mask layer, etching the second hard mask layer to form sidewall spacers on sidewalls of at the least one line in the first hard mask layer in the first region, wherein the minimum dimension of the at least one space in the first hard mask layer in the first region is reduced to a second critical dimension (A) less than achievable at the resolution limit of lithography; to form sidewall spacers on sidewalls of the at least one line in the second region; and etching the layer to form the line and space pattern in the first region corresponding to the first master line and space pattern in the first hard mask layer in the first region, wherein a space in the first region includes the second critical dimension (A) less than achievable by the resolution limit of lithography.

Claims Text - CLTX (4):

4. The method according to claim 1, further comprising the steps of: depositing an anti-reflective coating (**ARC**) on the first hard mask layer; **patterning the ARC** and the first hard mask layer to form a second master-line and space pattern therein, the second master line and space pattern includes lines and spaces including a minimum dimension achievable at the resolution limit of lithography; and depositing the second hard mask layer over the second master line and space pattern.

Claims Text - CLTX (5):

5. The method according to claim 1, further comprising the steps of: depositing, **patterning** and etching a first photosensitive layer to form lines and at least one space therebetween, the lines in the first photosensitive layer include vertical walls and the at least one space therebetween includes the minimum dimension (B) achievable at the resolution limit of lithography; and forming a first hard mask by transferring to the first hard mask layer a first patterned image of the first photosensitive layer by anisotropically etching the first hard mask layer to form therein lines and at least one space, the at least one space in the hard mask layer includes vertical walls and the minimum dimension (B) achievable at the resolution limit of lithography.

Claims Text - CLTX (7):

7. The method according to claim 5, further comprising the steps of: depositing, **patterning** and etching a second photosensitive layer over the substrate to form a second patterned image therein, comprising: masking the first region, and exposing the second region, and transferring to the layer the line and space pattern of an exposed portion of the first master line and space pattern of the first hard mask layer by anisotropically etching the layer to form at least one line therein in the second region, wherein the at least one line in the layer in the second region includes substantially vertical walls and the second critical dimension (B).

Claims Text - CLTX (13):

13. A method of **patterning** a layer on a substrate including a first region and a second region, the method comprising the steps of: providing a substrate including the layer to be patterned interposed between the substrate and a first hard mask layer to be patterned; coating the first hard mask layer to be patterned with a first photosensitive layer; **patterning** and etching the first photosensitive layer to form a first patterned image including lines and at least one space, the lines in the first photosensitive layer and the at least one space include substantially vertical walls and include a minimum dimension (B) achievable at a resolution limit of lithography; transferring to the first hard mask layer the first patterned image by anisotropically etching the first hard mask layer to form lines and at least one space, the lines and the at least one space in the first hard mask layer include substantially vertical walls and the minimum dimension (B) achievable at the resolution limit of lithography; coating the first hard mask layer with a second photosensitive layer; **patterning** and etching the second photosensitive layer to form a second patterned image including a mask over the first region and exposing the second region; etching the layer in the second region to form a line and space pattern therein including at least one line in the second region including the critical dimension (B) achievable at the resolution limit of lithography; depositing a conformal hard mask layer over the hard mask layer, exposed surfaces of the layer and exposed surfaces of the substrate; forming sidewall spacers on the vertical walls of the lines of the first hard mask in the first region whereby the minimum dimension (B) of the at least one space in the first region is reduced; forming sidewall spacers on the vertical walls of the at least one line in the second region; coating the substrate with a third photosensitive layer; **patterning** and etching the third photosensitive layer to form a third patterned image, wherein the first region is exposed and a remaining portion of the third photosensitive layer acts as a mask in the second region; etching the layer in the first region to form a line and space

pattern, wherein the at least one space in the layer in the first region includes a second critical dimension (A) less than achievable by the resolution limit of lithography.

US-PAT-NO: 6200857

DOCUMENT-IDENTIFIER: US 6200857 B1

****See image for Certificate of Correction****

TITLE: Method of manufacturing a semiconductor device without
arc loss in peripheral circuit region

----- KWIC -----

Abstract Text - ABTX (1):

Improved dimensional accuracy of the gate electrode structure in the peripheral circuitry region of a semiconductor device is achieved by avoiding ARC loss during photoresist stripping associated with plural maskings in the core memory cell region during patterning and ion implantations. Embodiments include initially etching to form the gate electrode structure in the peripheral circuitry region. Subsequently, processing in the core memory cell region is conducted by etching the stacked gate electrode structure and ion implanting to form the source/drains with attendant stripping of photoresist layers.

TITLE - TI (1):

Method of manufacturing a semiconductor device without arc loss in peripheral circuit region

Brief Summary Text - BSTX (5):

Semiconductor devices typically comprise a substrate and elements such as transistors and/or memory cells thereon. Various interconnection layers are formed on the semiconductor substrate to electrically connect these elements to each other and to external circuits. Conventional manufacturing techniques typically comprise forming memory cells in a core memory cell region and forming peripheral circuitry. Processing to form features peculiar to the core memory cell region does not usually correspond or is not necessarily optimal to processing for the peripheral circuitry region. For example, conventional methodology requires the use of at least three separate photoresist masks in the core memory cell region which are removed from the ARC overlying the gate electrode layer in the peripheral circuitry region prior to patterning the gate electrode structure in the peripheral circuitry region. Such conventional methodology requires the formation and removal of different photoresist masks for etching the stacked gate electrode structure, ion implanting impurities to

form shallow source/drain extensions and ion implanting impurities to form moderate or heavily doped source/drain implants. These photoresist masks are conventionally removed from the peripheral circuitry region prior to patterning the gate electrode structure of the peripheral circuitry region. However, each time the photoresist is stripped from the ARC, some of the ARC is lost, thereby altering its functional capabilities with respect to avoiding deleterious reflections during photoresist patterning. Consequently, a loss of critical dimension is encountered upon subsequent patterning of the underlying gate electrode structure.

Brief Summary Text - BSTX (6):

As miniaturization proceeds apace, the loss of dimensional accuracy, including in the peripheral circuitry region, becomes acutely problematic. Accordingly, a need exists for methodology enabling accurate patterning of a gate electrode structure in the peripheral circuitry region, notwithstanding the use of a plurality of masks in the core memory cell region which require stripping.

Brief Summary Text - BSTX (10):

According to the present invention, the foregoing and other advantages are achieved in part by a method of manufacturing a semiconductor device comprising a core memory cell region and a peripheral circuitry region, the method comprising the following steps: (a) forming a first gate electrode stack in the memory cell region, the first gate electrode stack comprising, sequentially: a tunnel dielectric layer; a charge storage electrode layer, e.g., a floating gate electrode layer; a dielectric layer; a control gate electrode layer, and an anti-reflective coating (ARC); (b) forming a second gate electrode stack in the peripheral circuitry region, the second gate electrode stack comprising, sequentially: a dielectric layer; a gate electrode layer; and an ARC; (c) depositing a first layer of photoresist material over the core memory cell and peripheral circuitry regions; (d) forming a first photoresist mask on the second gate electrode stack; (e) etching the second gate electrode stack, while the first gate electrode stack is masked by the first layer of photoresist material, to form a gate electrode structure comprising, sequentially: a gate dielectric; a gate electrode; and an ARC; (f) removing the first photoresist mask from the peripheral circuitry region and the first layer of photoresist material from the memory cell region; (g) forming a second photoresist layer over the core memory cell and peripheral circuitry regions; (h) forming a second photoresist mask on the first gate electrode stack; and (i) etching the first gate electrode stack to form at least one stacked gate electrode structure comprising, sequentially: a tunnel dielectric; a charge storage electrode; an intergate dielectric; a control gate electrode; and an ARC.

Brief Summary Text - BSTX (11):

Embodiments of the present invention include the further manipulative steps of: **removing** the second photoresist mask from the memory cell region and second layer of photoresist material from the peripheral circuitry region; depositing a third layer of photoresist material over the core memory cell and peripheral circuitry regions; forming a third photoresist mask over the core memory cell region; ion implanting impurities to form shallow source/drain extension implants associated with each stacked gate electrode structure; **removing** the third photoresist mask from the core memory cell region and third layer photoresist material from the peripheral circuitry region; forming a fourth photoresist mask over the core memory cell region and ion implanting impurities to form moderately or heavily doped source/drain implants. Subsequent processing includes annealing to activate the ion implanted regions.

Detailed Description Text - DETX (2):

The present invention addresses and solves the problem of **ARC** loss in the peripheral circuitry region prior to **patterning** the gate electrode structure as a result of plural photoresist stripping steps attendant upon forming the stacked gate electrode structure and source/drain regions in the core memory cell region. During conventional practices, the **ARC** in the peripheral circuitry region is degraded by virtue of stripping at least three layers of photoresist material, as with sulfuric acid with or without an oxygen plasma, to implement formation of transistors in the core memory cell region prior to **patterning** the gate electrode structure in the peripheral circuitry region. In accordance with embodiments of the present invention, the **gate electrode stack** in the peripheral circuitry region is initially etched to form a peripheral **gate electrode** structure before forming and **removing** photoresist layers attendant upon processing to form transistors in the memory cell region. Thus, the **ARC** in the peripheral circuitry region is not exposed to a single photoresist stripping step prior to **patterning** to form the gate electrode structure in the peripheral circuitry region.

Detailed Description Text - DETX (3):

After the gate electrode structure in the peripheral circuitry region is patterned, the stacked gate electrode structure in the memory cell region is formed by forming a photoresist mask and attendant stripping. Subsequently, the shallow source/drain extension implants and moderately or heavily doped source/drain implants are formed in the core memory cell region. The formation of such implants requires an additional two photoresist masks and attendant photoresist layer strippings. However, the stripping of photoresist material attendant upon formation of such ion implantation masks is conducted subsequent

to patterning the gate electrode structure in the peripheral circuitry region and, hence, does not adversely impact the integrity of the ARC prior to patterning, thereby improving the accuracy of the gate electrode structure in the peripheral circuitry region. Subsequently, annealing is conducted to activate the implants and the ARC is removed from the core memory cell and peripheral circuitry regions in a conventional manner, as with phosphoric acid.

Detailed Description Text - DETX (5):

An embodiment of the present invention is schematically illustrated in FIGS. 1-4, wherein similar features are denoted by similar reference numerals. As indicated, FIG. 1 illustrates a portion of a core memory cell region (core) and a peripheral circuitry region (periphery). As illustrated in FIG. 1, sequentially layers are deposited employing conventional deposition techniques resulting in the formation of a tunnel dielectric layer 20A and gate dielectric layer 20B on substrate 10. A charge storage electrode layer 21A and gate electrode layer 21B are then formed. Intergate dielectric layer 22 is then formed on the floating gate electrode layer 21A and can comprise silicon oxide, silicon nitride, or a conventional stacked silicon dioxide/silicon nitride/silicon dioxide (ONO) structure. Control gate electrode layer 23 is then deposited followed by deposition of ARC layer 24A and 24B typically at a thickness of about 200 .ANG. to about 350 .ANG.. The tunnel dielectric layer and gate dielectric 20A and 20B can comprise, for example, silicon oxide, while the gate electrode layers 21A, 21B and 23 can comprise doped polycrystalline silicon. The ARC layer can comprise any material conventionally employed as an ARC, e.g., silicon oxynitride. The first photoresist layer P1 is then deposited and the first photoresist mask M1 formed on the gate stack in the periphery.

Detailed Description Text - DETX (6):

Adverting to FIG. 2, the gate electrode stack in the periphery is first patterned, as by anisotropic etching, to form a gate electrode structure comprising gate dielectric 30, gate electrode 31, and ARC 32. The first layer of photoresist material P1 and first photoresist mask M1 are then stripped. Thus, ARC 32 in the periphery is not exposed to photoresist stripping before performing its anti-reflective function, thereby avoiding ARC loss and improving the dimensional accuracy of the patterned underlying gate electrode structure in the periphery.

Detailed Description Text - DETX (7):

As illustrated in FIG. 2, a second layer of photoresist material P2 is then deposited and a second photoresist mask M2 formed in the core overlying the gate electrode stack. The gate electrode stack in the core is then patterned,

as by anisotropic etching, as schematically illustrated in FIG. 3 to form a stacked gate electrode structure comprising tunnel dielectric 40, charge storage electrode 41, intergate dielectric 42, control gate 43, and ARC 44. The second photoresist mask M2 and second layer photoresist material P2 are then stripped.

Detailed Description Text - DETX (8):

As illustrated in FIG. 3, a third layer of photoresist material P3 is then deposited and a third photoresist mask M3 formed in the core. Ion implantation is then conducted to form shallow source/drain extensions 45. The third layer of photoresist material P3 and third photoresist mask M3 are then removed. As shown in FIG. 4, a layer of dielectric material P4, e.g., silicon dioxide, is then deposited and a fourth mask M4 is formed in the core. Fourth mask M4 comprises dielectric sidewall spacers, such as silicon dioxide, which serve as a mask during ion implantation to form moderately or heavily doped source/drain implants 50. Dielectric layer P4 and fourth mask M4 are then removed followed by removal of ARCs 44 and 42, as by employing phosphoric acid.

Detailed Description Text - DETX (10):

As illustrated in FIGS. 1-4, the gate electrode structure in the periphery is etched prior to being exposed to any photoresist stripping attendant upon transistor formation in the core. Accordingly, ARC loss due to photoresist stripping prior to patterning is avoided with an attendant improvement in the dimensional accuracy of the patterned underlying peripheral gate electrode structure. Conventional practices are more attentive to the requirements of the core memory cell region as it requires greater processing. Accordingly, conventional practices are traditionally focused upon completing processing in the core memory cell region prior to addressing the requirements of the peripheral circuitry region. However, the numerous photoresist stripping steps, e.g., typically about three, prior to patterning the gate electrode structure in the peripheral circuitry region results in a loss of ARC, thereby resulting in a loss of accuracy in critical dimensions of the features in the peripheral circuitry region, notably the gate electrode structure. This problem becomes particularly acute as feature sizes plunge into the deep submicron range. The present invention comprises a strategic sequence of manipulative steps wherein the gate electrode structure is etched in the peripheral circuitry region before exposure to any photoresist stripping, thereby avoiding ARC loss and, hence, improving the accuracy of the etched features in the peripheral circuitry region.

Claims Text - CLTX (2):

(a) forming a first gate electrode stack in the memory cell region, the

first gate electrode stack comprising, sequentially:

Claims Text - CLTX (7):

an anti-reflective coating (ARC);

Claims Text - CLTX (8):

(b) forming a second gate electrode stack in the peripheral circuitry region, the second gate electrode stack comprising:

Claims Text - CLTX (11):

an ARC;

Claims Text - CLTX (13):

(d) forming a first photoresist mask on the second gate electrode stack;

Claims Text - CLTX (14):

(e) etching the second gate electrode stack, while the first gate electrode stack is masked by the first layer of photoresist material, to form a gate electrode structure comprising, sequentially:

Claims Text - CLTX (17):

an ARC;

Claims Text - CLTX (18):

(f) removing the first photoresist mask from the periphery circuitry region and first layer of photoresist material from the core memory cell region;

Claims Text - CLTX (20):

(h) forming a second photoresist mask on the first gate electrode stack; and

Claims Text - CLTX (21):

(i) etching the first gate electrode stack to form at least one stacked gate electrode structure comprising, sequentially:

Claims Text - CLTX (26):

an ARC.

Claims Text - CLTX (29):

(j) removing the second photoresist mask from the core memory cell region and the second layer of photoresist material from the periphery circuitry region; and

Claims Text - CLTX (35):

(k.sub.4) **removing** the third photoresist mask from the core memory cell region;

Claims Text - CLTX (37):

(k.sub.6) implanting impurities, employing the fourth mask, to form moderate or heavily doped source/drain implants associated with each stacked **gate electrode stack**;

Claims Text - CLTX (38):

(k.sub.7) **removing** the fourth mask; and

Claims Text - CLTX (44):

(k.sub.4) comprises **removing** the third layer of photoresist material from the peripheral circuitry region; and

Claims Text - CLTX (45):

(k.sub.7) comprises **removing** the fourth layer of photoresist material from the peripheral circuitry region.

Claims Text - CLTX (50):

9. The method according to claim 1, wherein the **ARC** comprises silicon oxynitride.

DERWENT-ACC-NO: 2001-290769

DERWENT-WEEK: 200330

115 6,235,587

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TITLE: Manufacture of semiconductor memory device with
antireflective coating

----- KWIC -----

Basic Abstract Text - ABTX (1):

NOVELTY - Improved dimensional accuracy of the gate electrode structure in the periphery circuitry region of a semiconductor device is achieved by reducing anti-reflective coating (ARC) loss during photoresist stripping associated with a mask formation in the core memory cell region during patterning and ion implantations.

Basic Abstract Text - ABTX (3):

(1) forming a first gate electrode stack in the memory cell region, the first gate electrode stack comprising a tunnel dielectric layer, a charge storage electrode layer, a dielectric layer, a control gate electrode, and an anti reflective coating (ARC);

Basic Abstract Text - ABTX (4):

(2) forming a second gate electrode layer, and an ARC;

Basic Abstract Text - ABTX (6):

(4) forming a first photoresist material on the first gate electrode stack;

Basic Abstract Text - ABTX (7):

(5) etching the first gate electrode stack, while the second gate electrode stack is masked by the first layer of photoresist material, to form at least one stacked gate electrode structure comprising a tunnel dielectric, a charge storage electrode, an intergate dielectric, a control gate electrode, an ARC;

Basic Abstract Text - ABTX (9):

(7) forming a second photoresist mask on the second gate electrode stack;

Basic Abstract Text - ABTX (10):

(8) etching the second gate electrode stack to form a second gate electrode structure comprising a gate dielectric, a gate electrode, an ARC.

Basic Abstract Text - ABTX (20):

ARC layer 24A, 24B

Title - TIX (1):

Manufacture of semiconductor memory device with antireflective coating

Equivalent Abstract Text - ABEQ (1):

NOVELTY - Improved dimensional accuracy of the gate electrode structure in the periphery circuitry region of a semiconductor device is achieved by reducing anti-reflective coating (ARC) loss during photoresist stripping associated with a mask formation in the core memory cell region during patterning and ion implantations.

Equivalent Abstract Text - ABEQ (3):

(1) forming a first gate electrode stack in the memory cell region, the first gate electrode stack comprising a tunnel dielectric layer, a charge storage electrode layer, a dielectric layer, a control gate electrode, and an anti reflective coating (ARC);

Equivalent Abstract Text - ABEQ (4):

(2) forming a second gate electrode layer, and an ARC;

Equivalent Abstract Text - ABEQ (6):

(4) forming a first photoresist material on the first gate electrode stack;

Equivalent Abstract Text - ABEQ (7):

(5) etching the first gate electrode stack, while the second gate electrode stack is masked by the first layer of photoresist material, to form at least one stacked gate electrode structure comprising a tunnel dielectric, a charge storage electrode, an intergate dielectric, a control gate electrode, an ARC;

Equivalent Abstract Text - ABEQ (9):

(7) forming a second photoresist mask on the second gate electrode stack;

Equivalent Abstract Text - ABEQ (10):

(8) etching the second gate electrode stack to form a second gate electrode structure comprising a gate dielectric, a gate electrode, an ARC.

Equivalent Abstract Text - ABEQ (20):

ARC layer 24A, 24B

Standard Title Terms - TTX (1):

MANUFACTURE SEMICONDUCTOR MEMORY DEVICE ANTIREFLECTIVE
COATING